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Statistical Analysis for Memristor Crossbar Memories

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The inherent memory capabilities bound with compactness and scalability features pose the memristor as an ideal rival for conventional non-volatile memories. Its use within a crossbar structure offers high-density storage and tight dimensionality. A fitting parameter in the midst of the trend towards nanoscale integration, where gateless memories are on the rise in an attempt to achieve further space savings. Nonetheless, the gate sacrifice comes at the expense of the fidelity and accuracy of the readout values. In which the sneak path phenomenon distorts the data and acts as a hindering factor to reliable detection and higher density attainment. In this work, a novel approach is adopted to accommodate the sneak path and counter its effect on the memory reading. In contrast to the alternative techniques, where spatial and temporal solutions are applied to alleviate the distortion limitation and set a dynamic threshold, statistical measures benefit from the prior read data within the array. It builds upon the noise reduction and estimation principles, mainly borrowing concepts of coding and detection theory to enhance the access time and accuracy of the reading process.

Keywords: Channel coding, crossbar array, detection theory, memristor, noise estimation, sneak path

1 INTRODUCTION

Non-volatile memories regarding the SRAM/DRAM and flash constituents suffer from leakage either in terms of the charge or resistance drift due to

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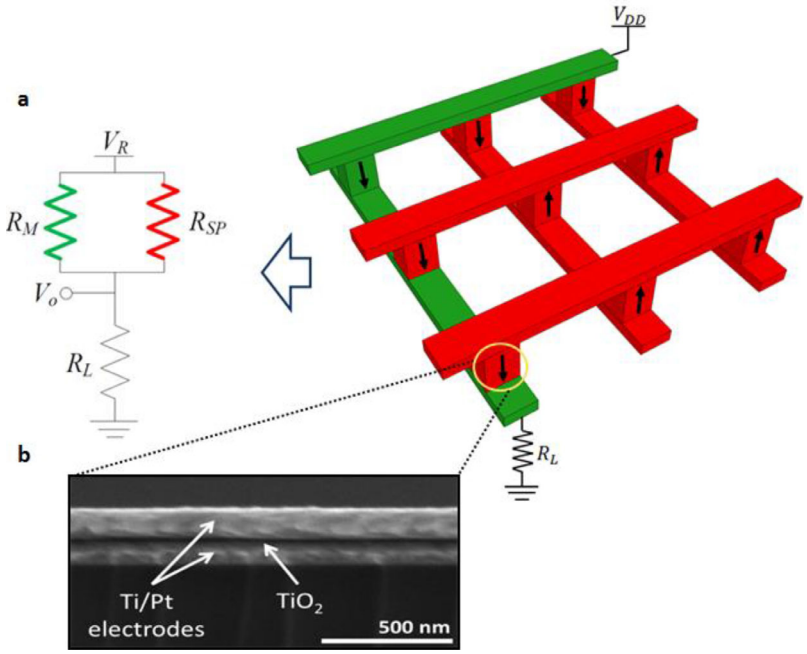

FIGURE 1
Sneak Path in Memristor-based Memories (a) Crossbar array with the sneak path formation and the corresponding equivalent read circuitry. **(b)** Cross-section of the scanning electron microscope of fabricated memristor devices [28].

the intrinsic nature of its internal components [24, 25]. On the other hand, resistive RAMs (RRAM), in which memristors act as the storage elements, offer a more stable alternative where the values are retained over time without the risk of drifting [4, 6]. A feature owing back to the basic operation principle of memristors in which the low resistance state (LRS) and the High resistance state (HRS) of the cell are attained through threshold switching. A state switching within the memristor is triggered once the applied input bias exceeds a set threshold value [3, 22, 23]. Thus eliminating the risk of any shift in the actual data values saved. Despite this sustainability, and however observed in a different situation, leakage remains to be a problem as it is present during the read-out operation. Memristor-based memories have mainly crossbar structures in which the memristor resides at the intersection of two perpendicularly crossing nanowires [2, 10, 27] as shown in Figure 1b. Resistive sensing is usually applied to read the value of the cell. In standard architectures, this operation requires the activation of the cell row where a voltage is applied at its edge, and grounding is set on the selected column respectively while leaving the remaining parts of the array floating [16].

In gateless memories, where no switch is available at the gate of the cell, the activation process will affect all the cells in the selected row and column, and additional paths are formed within the array [2, 27]. A phenomenon addressed as the sneak path is then encountered where the current leaks through the non-primary path and acts as a parallel resistor to the cell resistance intended for reading as shown in the array and corresponding equivalent circuit in Figure 1a. To that end, and in spite of the validity of the stored data, an added distortion imposed by the sneak path resistance diverts the readings from its actual quantity compromising by that the reliability and accuracy of the reading process [5, 8]. Diverse solutions were provided in an attempt to overcome the un-clear threshold setting, architectural techniques concentrate on overriding the leakage through incorporating alternative cross point elements [7,9,15,17,20]. Otherwise, temporal and spatial techniques [16, 26] are used to override the leakage. In one scenario, the actual value is read, and since no clear threshold between the high and low values in the memory is available, the one value is written and then read, followed by a writing of the zero value and reading again, finally a comparison between the actual read value and the two written values for the on and off states [16]. Corresponding thus to an average of five to six steps process in order to decode a single bit, not to mention the writing incorporated as well, that would shorten the lifetime of the memory [21, 23]. On the other side, a small architectural modification in the array structure, where the unselected rows and the columns are grouped, creates additional nodes for reading the resistances. Moreover, it reduces the reading process into three steps using different points and eliminates any writing operation to the memory [26]. However practical and appealing these solutions may seem, the access time is the primarily affected parameter in both cases. In this paper, the memory array is dealt with as a communication medium with added noise that actually corresponds to the sneak path distortion. Principles applied to combat the noise and reach an enhanced detection are utilized in the memory system to achieve a better reliability and reduce the effect of the noise to the best extent with no modification required and a faster access time. Similar approaches induce isolating points within the memory to virtually split the array into smaller sizes [18–20]. The read margins improvement was attained at the expense of fabrication with different material for the isolating points as well as the density of the array. While our encoding scheme proposed benefits from the high resistance state of the memristor to dampen the effect of the sneak path with no added complexity to the fabrication process. Furthermore, an alternative technique building on inserting reference points was introduced in [12]. Alternating high and low reference points were used to set the threshold between the two reference points per fragment. To that end, the noise was assumed to be one dimensional and dynamic threshold setting was

constantly required for enhancing the accuracy of the readout operation. In contrast, the pilot scheme proposed build on estimation principles for the distortion and takes into account the correlation of the noise along the horizontal and vertical read lines respectively.

The introduction depicted in Section one provides a brief overview of the non-volatile memory status and the state of the art solutions to gateless memristor memories. Section two deals with the analysis of the sneak path and the noise analogy to the communication systems. The coding scheme or the zero padding application and its consequences on the readout process are discussed in Section three, and Section four introduces the noise estimation techniques and its potential practicality on the array. Finally, the paper is concluded with a summary of the overall concepts along with the resultant aftermath of the adopted principles.

2 NOISE ANALYSIS

In a Synopsys HSPICE based experimental setup, crossbar memristor-memories were simulated. The simulations accounted for the crossbar nanowires resistance (R_{cb}) as an added imperfection that would be faced in a fabricated circuit environment. Moreover, and in order to facilitate the testing process and allow for further flexibility in the design and a broader range of possibilities, a python script was created to generate the SPICE netlist. The netlist incorporated the complete crossbar resistance along with the memristance values and the read input voltage setting as well. This flexibility in the design paved the way for faster and more elaborate simulations, a wider set of test data inclusion, and detailed analysis for several array parameters. To that end, data inputs were saved in the array in the form of resistance, where the memristor values corresponding to '1' were mapped to the R_{ON} resistance, and the '0' to the R_{OFF} resistance covering by that the two extremes of the resistance range and the data as well. Theoretically, in the absence of noise or distortion added, the read-out values should correctly map to the write in quantities.

However, this is not the case for the readings of the memristor memory. Our HSPICE simulations showed an added impurity imposed by the sneak path that shifted the numbers from their initial values. Several array sizes were simulated starting from a 64x64 array up to 512x512. The distribution of the sneak path or interference was found to fit a Gaussian model with readouts that are almost closely overlapping for the R_{ON} and R_{OFF} values [13]. The overlap increased in severity with the larger size of the array. The probability density function $p(x)$ of the Gaussian distribution is described as

$$p(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{-(x-\mu)^2}{2\sigma^2}} \tag{1}$$

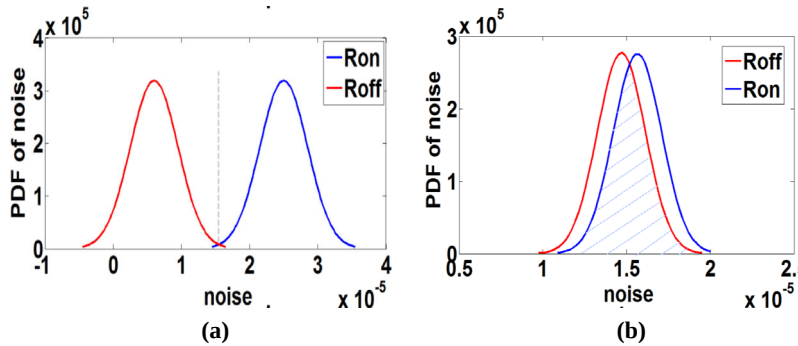

FIGURE 2

Noise Spectrum (a) Ideal State for the distribution of the high and low bits in the absence of the noise. **(b)** Spectrum for R_{ON} and R_{OFF} values showing the overlap in the distributions, where the shaded region corresponds to the error probability.

where μ stands for the mean value of R_{ON} or R_{OFF} respectively. Moreover, the spectrum of the high and low values is depicted in Figure 2, where the two distributions are quite overlapping with no clear-cut to set a threshold that would ensure an accurate and reliable readout process. Building upon the standard communication principles, in terms of channel coding and estimation, and integrating them within the array would enhance the performance and result in a wider separation of spectrums. All of which would come into the benefit of the probability of error that would be diminished and consequently adhere to the fidelity and accuracy requirements.

3 ARRAY CODING

In communication terms, noise and added imperfections in the channel result in the degradation of performance and higher probabilities of error. One way to combat these added impurities is by increasing the power of the signal to be greater than that of the noise and thus getting the decision regions further spread apart and forming a clear-cut threshold for detection. However, this would not be applicable in our case as the noise and the signal are both originating from the same source, which is the cross-point device resistance along the activated columns and rows. Thus, increasing the voltage would consequently increase the sneak path resistance or the noise model. On the other hand, incorporating channel coding schemes, that are inherently tailored for combating the noise, would result in reducing the distortions while keeping the input signal intact. It adds some redundancy to the transmitted bits, decreasing by that the actual information bits sent over the channel. This concept of channel encoding could also be incorporated in the memristor-based memory, particularly in the situation of the read-out, where the saved bits act

as the transmitted data, and the sneak path in the remaining part of the memory is the channel itself that would add the noise factor to the read-out bits. As the current is measured to detect the stored information, the higher the resistance in the sneak path, the lower is the current consequently leading to a much less deviation. Building upon these ideas, the concept of zero padding is applied. As zero corresponds to the R_{OFF} value of the memristor, adding more zeros would have kind of a blocking effect on the leakage current and a guarding siege around the read-out bit. The R_{OFF} value basically acts as a damping resistor to the altering resistance.To measure the efficiency of the applied technique, the probability of error was chosen as a figure of merit. It corresponds to the shaded region depicted in Figure 2b. The array of high and low values corresponding to 1s and 0s holds a close resemblance to the binary shift keying (BPSK) modulation scheme. Thus, the error probability sums up to the miss interpretation of a bit with its opposite value. That is the mix between an ROn value where an R_{OFF} value is actually saved, and vice versa. Equations 2 to 4 show the conditional error probabilities for R_{ON} and R_{OFF} values respectively [14] where xth corresponds to the intersection point between the two spread spectrums. The conditional probability is then calculated based on the Q function for the Gaussian distributions.

$$P_{e/b1} = P\{decoding(b_1/b_0)\} = P\{x_{b_1} < x_{th}\} \tag{2}$$

$$P_{e/R_{ON}} = 1 - Q(\frac{R_{th} - \mu_{R_{ON}}}{\sqrt{var(R_{ON})}}) \tag{3}$$

$$P_{e/R_{OFF}} = 1 - Q(\frac{R_{th} - \mu_{R_{OFF}}}{\sqrt{var(R_{OFF})}}) \tag{4}$$

The total error probability is then calculated as follows

$$P_e = P(R_{ON}).P_{e/R_{ON}} + P(R_{OFF}).P_{e/R_{OFF}} \tag{5}$$

However, since mainly random data is stored in the array, the number of high and low values is equiprobable. Thus, the error probability is reduced to

$$P_e = \frac{1}{2}(P_{e/R_{ON}} + P_{e/R_{OFF}}) \tag{6}$$

The decrease in the error probability directly maps to the enhancement in the detection process attained. Nonetheless, a compromise is present between the accuracy of the read operation and the density of the memory. As the zero padding would acquire some of the actual data bits positions and fill it

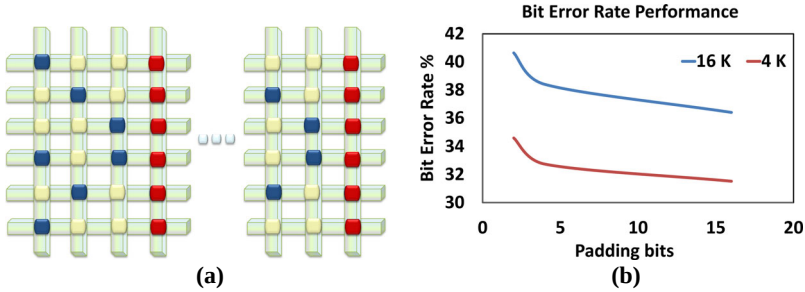

FIGURE 3
Memristor-based Memory Coding (a) Padding the array with zeros or high resistance R_{OFF} in preset columns (red dots) depending on the coding scheme. **(b)** The bit error rate performance in response to the applied padding bits and array sizes

with zeros. Thus, with more padding the density would be further reduced. Figure 3b summarizes the achieved results for different array sizes in terms of the bit error rate. SPICE-based simulations of the complete crossbar were conducted with a different number of padding bits (Figure 3a). The memristor elements in the padding locations within the array were set to a high resistance of R_{OFF}. Simulations for 64x64 or 4K and 128x128 or 16K show the tighter decision regions and higher noise effect with larger array dimensions. Reading out from the array was based on floating rows and column scheme (FRC). A read voltage of 1V was applied consecutively to every data crosspoint in the array. That is excluding the padding bits. The output current was then measured at the column terminal of the bit being read. These simulations were run over several data distributions for the 4k and 16k arrays respectively. The read margin was then calculated as the difference between the minimum R_{OFF} and maximum R_{ON} values respectively. An improvement of merely 5% was attained with respect to threshold regions and their proximity measures. These minor improvements reflect the shorting of the coding scheme applied. It does not fully utilize the information that could be extracted from the array itself; where the padding bits are simply used as damping points rather than estimation hubs. Further analysis and a priori estimation and compensation factors are proposed to help reduce the noise effects.

4 ESTIMATION SCHEMES

Dealing with the memory array as a communication channel imposes the applicability of characterization principles to achieve a reliable detection level. As noise estimation and equalization are crucial for overriding the distortions and mapping the data to its correct equivalent values. In one format,

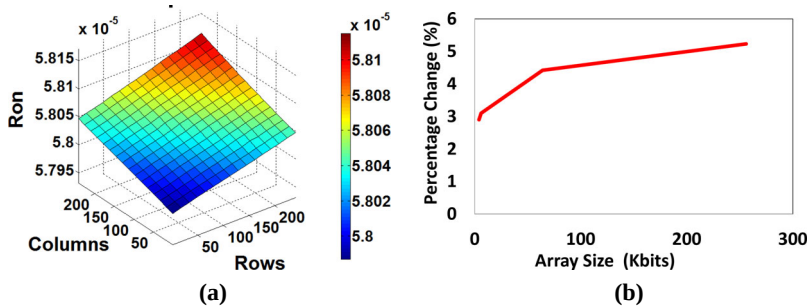

FIGURE 4

Bit Location Effect (a) Percentage variation of the R_{ON} value across the bit location in the array for a checkered data set. **(b)** The average percentage change of the R_{ON} with respect to the array size. The square array sizes ranged from 1Kb to 256Kb.

the noise could be split into two major components, deterministic and random. Deterministic noise refers to the static effects that encounter the signals through its propagation due to its location throughout the transmission. Whereas the random noise corresponds to the white, time variant, and mostly data dependent variations added to the signal [14]. In the case of the memory array, the bit location effect and the data related random noise are studied in the following subsections to analyze their individual contributions to the degradation of the accuracy of the read-out values.

4.1 Bit Location Effect

The most prominent effect governing the location dependence is the activation process. The read lines are activated at the beginning of the rows and columns to be read. Thus, the distance of the desired bit from the reading points would have an effect on the values extracted out of the array [1, 12]. The testing and validation of the above hypothesis were based on a checkered input simulation. It accounted for a balanced set of the data to characterize the crossbar effect irrespective of the data within. Figure 4a shows the delta variation for a square array of 256×256. The delta ranged to a maximum of 3%, with increasing ranges as the dimensions increase but still confined to a limited factor as depicted in Figure 4b. It ended up showing that the memory could be dealt with in a sphere like fashion, whether close or far away from the reading points, the location has a minor effect that could be incorporated into the estimation.

4.2 Pilot Assisted Estimation

Triggered by the reuse capabilities and a priori estimation, a pilot based technique was adopted to measure the noise parameters. To that end, the array was tainted with predetermined values, mainly R_{OFF} to reduce the effect of

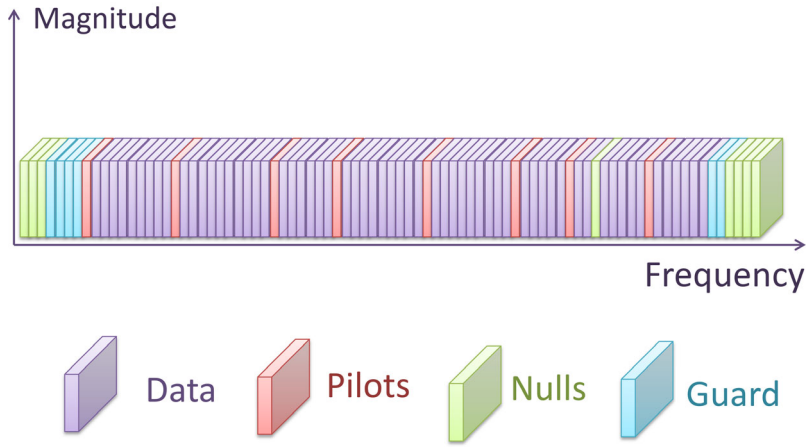

FIGURE 5
Pilots in Communication Original use of reserved slots in communication systems for a predetermined data set to allow for channel estimation and the distortion undergone throughout the transmission.

the sneak path current. Building upon borrowed principles from channel estimation and equalization, pilots are used to have an estimate of the transfer function of the channel, as depicted in Figure 5. Based on the validity of the estimate and the variation interval for the medium, the number and modeling requirements are established [11]. The noise values were calculated from the difference between the output values read and the input bits written. Signal processing techniques are used to form an analytical relation between the close sets of pilots and the estimated bits. The noise values are randomly distributed per cell. Nonetheless, a strong correlation is present between the row and column parameters of the target cell [13], as shown in Figure 6a.

Based on these correlations, the pilots are set at the central diagonal of the array. Its setting is aimed to incorporate the two-dimensional feature of the noise parameter. Two adjacent pilots are used to compute an approximate evaluation of the noise factor at the cell lying across the horizontal and vertical direction of the pilots respectively. That is, elements at a particular row i are served by the pilot at cell (i,i) as its horizontal component and by the center element (j,j) as its vertical component, where j corresponds to the column the target cell resides in. A linear fitting algorithm is applied before the read operation to quantify the extent of contribution integrated within the pilot cell per each dimension. Thus, depending on whether this reference point is used as a horizontal or vertical factor to the noise estimation, a particular weight is applied to it. The weights are estimated a priori to the readout operation by considering the cells at the upper and lower diagonals to the pilots, and split-

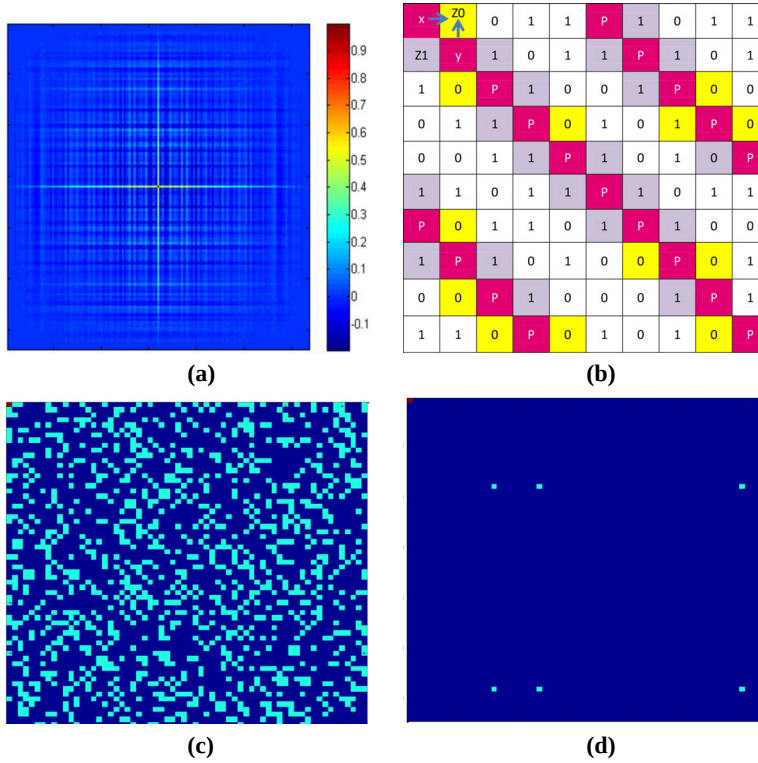

FIGURE 6

Estimation Scheme (a) The correlation among the vertical and horizontal noise parameters of the array. **(b)** The added diagonal pilots induced into the memory array. **(c)** The memory readout operation and error with a fixed threshold setting. **(d)** The enhanced readout, almost error free, after the application of the estimation technique with the induced pilots.

ting them into two sets of high and low values accordingly. In a mathematical format, the fitting algorithm is represented with the following parameters and equations.

$\{Z_v\}_{v=1}^{N}$ where Z_v corresponds to the number of interference observations, elements directly placed on the upper and lower cells adjacent to the pilot diagonal.

X_v corresponds to the same row interference neighbor, pilot at the same row of the observation cell.

Y_v corresponds to the same column interference neighbor, pilot at the same column of the observation cell

$$Z_v = \alpha X_v + \beta Y_v + \delta_v \tag{7}$$

where α and β are the weight factors that needs to be estimated, and δ is the error element induced quantifying the extent of the estimation parameters matching the actual observation. To that end, converting to the matrix format leads to the representation of the parameters X, Y, and Z to

$$Z = \begin{bmatrix} Z_1 \\ Z_2 \\ . \\ . \\ Z_N \end{bmatrix}, \psi = \begin{bmatrix} X_1 & Y_1 \\ X_2 & Y_2 \\ . & . \\ . & . \\ X_N & Y_N \end{bmatrix}$$

and the estimation parameters

$$\theta = \begin{bmatrix} \alpha \\ \beta \end{bmatrix}; \delta = \begin{bmatrix} \delta_1 \\ \delta_2 \\ . \\ . \\ \delta_N \end{bmatrix}$$

Equation 7 is consquently transformed into

$$Z = \psi\theta + \delta \tag{8}$$

The main objective is to minimize the error parameter δ, in which case, the weighted factors would fit perfectly the formulation presented in equation 8. An optimization based on minimum mean square error is adopted, leading to the conditions presented in equation 9.

$$\delta^T\delta = ||Z - \psi\theta||_2^2 \tag{9}$$

The corresponding optimization problem is solved by ensuring the values of θ to be set according to equation 10.

$$\hat{\theta} = (\delta^T\delta)^{-1}\psi^T Z \tag{10}$$

The linear fitting over a set of arrays with different data distributions split the effect equally between the vertical and horizontal components. Thus, the noise estimated from the diagonal pilot was split equally across the vertical and horizontal dimensions. Nonetheless, the coherence interval, or the validity of the noise estimate over several data points, is a further parameter to be considered. The estimate of the array noise was highly matched in the vicinity of the neighboring cells of the pilots. The further the data cell is from the

pilot, the lower is the accuracy of the reading. Thus, instead of having only the central diagonal assigned for pilots, further diagonal elements were set to pilots as well, as shown in Figure 6b. In that mode, the added diagonals aid in achieving higher accuracy for the readout operation. Thus, a proficient implementation of the pilot setting takes into consideration the compromise between the density and the number of pilots used. For that, a setup that serves the surrounding bits in the most efficient manner needs to be established to minimize the probability of error while keeping the density loss at its minimal.

Figures 6c and 6d show the average readout from a set of 64x64 arrays. The light points show an error in the reading while the darker points reflect correctly detected values. With a fixed threshold reading that does not employ any estimation technique, the error was spread all over the array and reached around 48%. On the other hand, with the pilot assisted read operation, the read out values were exact for almost the complete array. Furthermore, the error in the readout operation was reduced to less than 1%. The proposed estimation technique aims to benefit from the array data to inherently combat the noise while preserving a balance between the stringent requirements of accuracy and speed of access.

5 CONCLUSION

A statistical approach to deal with the sneak path problem was introduced, in which principles applied in communications systems helped alleviate some of the noise burden encountered. Channel coding offered minor improvements to the accuracy of the read-out values. However, noise decomposition provided a larger insight into the bit location effect and how the crossbar resistance could be of importance in the reading process. Finally, the incorporation of pilot bits allowed for noise estimation for values in the vicinity of the set bits. A note to the trade-off measure in which an evaluation metric needs to be put into activation for the proper choice of numbering and position of the preset values. Density versus accuracy, a newly added dimension to the requirement bundle, is a contrasting measure that needs to be tackled and optimized in order to yield a feasible solution.

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