Macrothink Institute™

Network Protocols and Algorithms
ISSN 1943-3581
2012, Vol.4, No.1

Low complexity FEC Systems for Satellite Communication

Ashwani Singh

Navtel Systems

2 Rue Muette, 27000,Houville La Branche, France

Tel: +33 237 25 71 86 E-mail: ashwani.singh@navtelsystems.com

Henry Chandran

Navtel Systems

2 Rue Muette, 27000,Houville La Branche, France

Tel: +33 237 25 75 14 E-mail: henry.chandran@navtelsystems.com

Received: January 31, 2012 Accepted: May 16, 2010 Published: May 30, 2010

DOI: 10.5296/npa.v4i1.1341 URL: http://dx.doi.org/10.5296/npa.v4i1.1341

Abstract

In order to address low power, low processing delay requirement of emerging satellite communication systems, there is a need for low complexity small block length forward error correction (FEC) codes. Furthermore the new trends towards the convergence of wireless and satellite terminals would also mean co-existence of support for very short and the long blocks of data in the same device. In this context a novel next generation high performance 4K low density parity check (LDPC) code is introduced in the paper. The error performance results for the proposed code are presented showing significant improvement of performance/complexity metrics over existing FEC systems.

Keywords: Forward error correction (FEC), Low Density Parity Check (LDPC) codes, Satellite Communication, Low power.

1. Introduction

In communication systems FEC coding improves data reliability by introducing redundant information into a data sequence prior to transmission, which enables a receiver to detect and possibly to correct errors without requesting retransmission of the original information. There are many FEC codes widely used in satellite communication like Reed-Solomon (RS), product codes, convolutional codes, turbo and low density parity check (LDPC) codes. However the next generation satellite communication systems e.g. digital video broadcast satellite/terrestrial (DVB-S2/T2) have readily adopted LDPC code for FEC [1], [2], mostly due to its near Shannon performance at very low signal to noise ratio [3].

For LDPC codes ”Code Dimensions” in terms of information word and codeword size may be in the order of hundreds or thousands digits (from 600 up to 64000 bits) resulting in large processing delays at low data rates. The cost of the hardware required for the iterative decoding and large block sizes can be significantly high for high data rates. Additionally, to improve the error correction performance of the LDPC codes a outer BCH code is concatenated to the LDPC code, which helps in lowering the error floor. The complexity of decoding the BCH at the receiver is not negligible, and the complexity increases with the error correction capability thus increasing the power consumption and overall processing latency. These factor demands innovative LDPC code design and their implementation, which has low error floors without the need of concatenation. Proposed next generation 4K LDPC codes are designed keeping this in mind.

In [4] authors have proposed very short frames 4K LDPC codes to be used in the return link of DVB-RCS+M (Return Channel via Satellite) system. However designed code still uses BCH to remove errors due to trapping set at the error floor, which results in increased implementation complexity. In [5] Trellis Ware have proposed a class of flexible LDPC codes which is defined by a sparse parity check matrix and the corresponding Tanner graph but is designed in a manner more similar to parallel concatenated convolutional codes (PCCCs) and serial concatenated convolutional codes (SCCCs). Various code length including 4K are supported with interesting performance results, however the propriety code construction method is a bottleneck for their effective adoption.

The rest of the article is organized as follows: Section II provides the overview of LDPC codes and its decoding algorithms. Section III gives the system overview of FEC used in typical satellite communication systems along with its different design parameters. Section IV present the next generation small LDPC codes and its error performance results and finally the paper concludes with section V giving some future perspectives.

2. LDPC Coding and Decoding

Low Density Parity Check (LDPC) Codes, are a class of linear block codes, with parity-check matrices H very sparse, i.e. the number of 1’s are small percentage of the zero elements [3]. R. Gallager defined an (N, m, n) LDPC code as a block code of length N having a small fixed number (m) of ones in each column of the parity check matrix H, and a small

fixed number (*n*) of ones in each rows of *H*. For ease of implementation, most of these codes in fact, are based on blocks of sub-matrices obtained by permutations of the rows of identity matrices leading to the so-called quasi cyclic (QC) codes [6].

2.1 Tanner Graph Representations

LDPC decoder architecture is strictly related to the Parity-Check Matrix H; in fact, due to the sparseness of this matrix, the decoder can be represented in term of a bipartite graph called Tanner Graph [7]. A bipartite graph is a graph where the elements of a first class can be connected to the elements of a second class, but not to the same class. In a Tanner graph for binary LDPC codes (Fig. 1 left half) there are two classes of Processing Elements (PEs) that are related to the rows and columns of the H matrix.

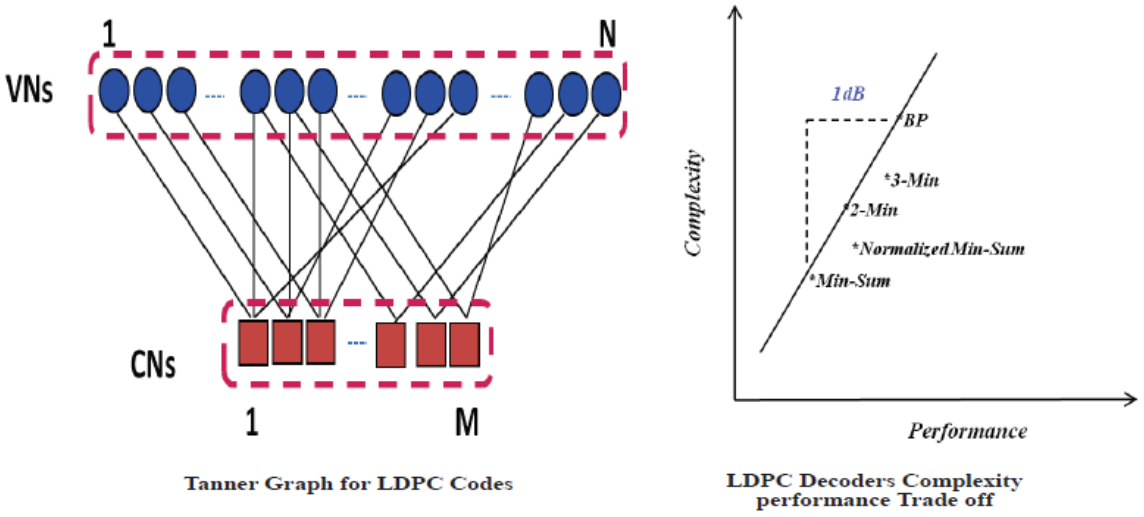

Figure 1. LDPC codes and Decoders.

The N nodes related to the rows, i.e. the length of the codeword also known as ”code-block”, are usually reported, in LDPC notation, as Variable (or Bit) Nodes (VNs); on the other hand, there are M = N-K nodes (K is the information word size), called Check Nodes (CNs) that are related to the columns of the H matrix, i.e. the M parity check equations of the code. Moreover, an edge e_{ji} on the Tanner Graph connecting a Variable Node VN*j* with a Check Node CN_i (i.e. messages exchanged between this two nodes) corresponds to a ”1” in the H matrix between row *j* and column *i*. The Tanner graph representation of error correcting codes is very useful since their decoding algorithms can be explained by the exchange of information along the edges of these graphs.

2.2 Decoding Algorithm

LDPC decoder architecture is strictly related to the Parity-Check Matrix H; in fact, due to the sparseness of this matrix, the decoder can be represented in term of a bipartite graph called Tanner Graph [8]. A bipartite graph is a graph where the elements of a first class can be connected to the elements of a second class, but not to the same class. In a Tanner graph for binary LDPC codes (Fig. 1 left half) there are two classes of Processing Elements (PEs) that are related to the rows and columns of the H matrix.

Right hand side of the Fig. 1 shows different algorithms for LDPC decoder implementation. BP based implementation involves addition operation and look up table (LUT). The Min Sum (MS) Algorithm is an area efficient, sub optimal approximation to the BP and was proposed by authors in [9]. There are different variant of this algorithm that were proposed later on, like 2 min method, which exploits the fact that in min-sum decoding out of all CN log likelihood ratios (LLRs) of a CN only two magnitudes are of interest, since only the minimum and the second minimum magnitude (2MIN) is used to produce LLRs for connected VNs. It is the natural way to compress data in memory and normally results in significant memory saving in CN kernel. There are other similar approaches in this class like λ-min [10]. As seen in the Fig. 1 higher is the sub optimality of chosen algorithm the error correction performance of the decoder degrades, however such suboptimal implementation do provide low complexity hardware for low power applications.

3. FEC Subsystem Design Space

Fig. 2 shows an example of fixed satellite broadcasting system, which uses LDPC codes for FEC. In the transmitter, redundancy bits are added to the user frame by encoder blocks of FEC sub-system. This new data stream is then mapped on to symbols using modulation techniques like QPSK, 8PSK, 16 APSK and 32APSK. On the receiver side De-Mapper LLR unit computes the LLRs and saves it in internal memory. The saved frames are iteratively decoded by the LDPC core unit and transmitted to the BCH decoder.

It should be noted that the high error correction performance of LDPC codes is not without its limitation; especially the performance of these codes suffers significantly from high error floors. Small residual error patterns may appear at the output of the LDPC decoder usually leading to high error floors, and are due to either low-weight codeword or the so-called trapping sets [11]. This error floor phenomenon appears generally between frame error rates (FER) of 10^{-4} and 10^{-6}, which is insufficient to reach present day QoS requirements for certain satellite communication systems like digital video broadcast for high definition television (HDTV). An effective code construction strategy could be employed to mitigate this issue; however some communication standards include BCH code concatenation to deal with the trapping sets problem [1], [2].

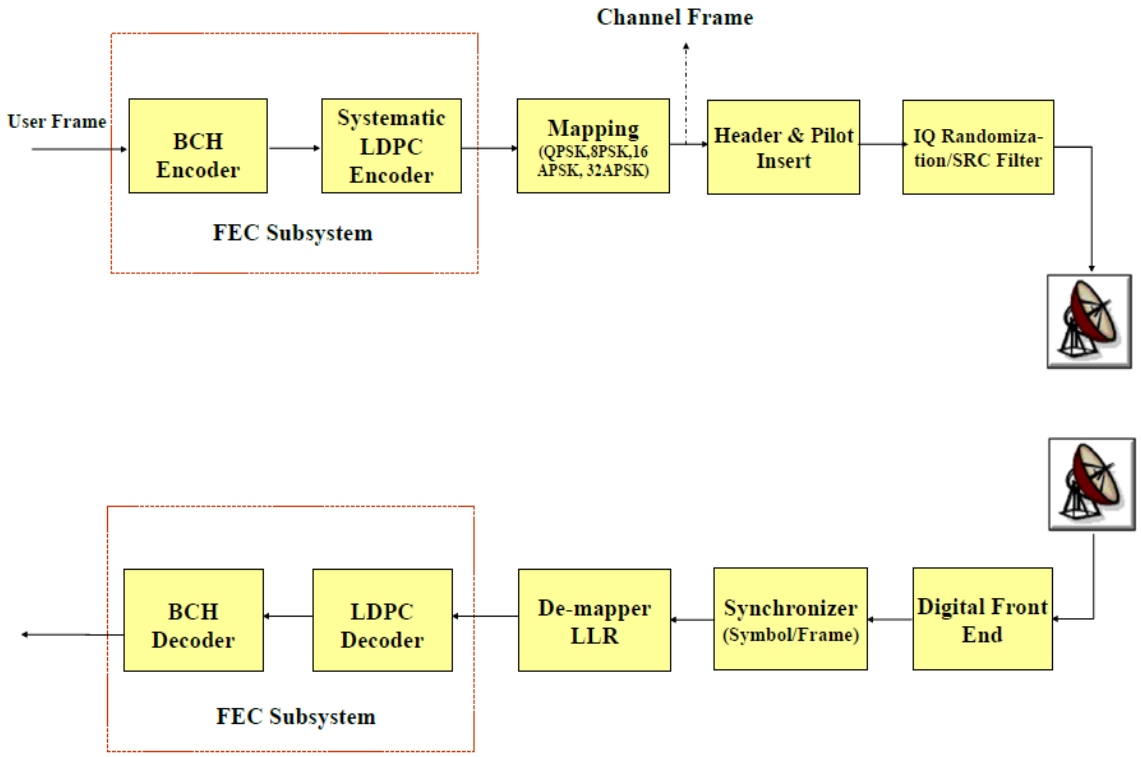

Figure 2. FEC System Model for Satellite Communication.

The categorization of a good FEC sub system depends mostly on what is important for the system under consideration i.e. the priorities of the chosen application where it is intended to be used. However an objective assessment of such systems could be performed based on following three metrics:

3.1 Error Correction Performance

The principle of Bit Error Rate (BER) or Frame Error Rate (FER) estimation with the Monte-Carlo (MC) simulation is well known: first fix the SNR of the simulation to determine the value of the standard deviation of the white Gaussian noise in the channel, then generate a modulated codeword, add the white gaussian noise and perform the iterative decoding algorithm to compute the A Posteriori Probability (APP) of the codeword symbols. Finally, based on APP, take a decision on the decoded symbols. If uncoded and decoded codeword differ, compute the number of errors. For the LDPC code this error correction performance could be split in two parts:

3.1.1 Waterfall Error Performance

Frame error rates of around 10^{-2}, 10^{-3} at the lowest possible signal to noise ratio (SNR).

3.1.2 Error Floor Performance

Low frame error rates of around 10^{-5} to 10^{-7} at the lowest possible signal to noise ratio

(SNR) guaranteeing a certain error correction capability. It is in reality a complimentary metric to the waterfall error performance i.e. codes with low error floor will normally have a poor waterfall performance.

3.2 Implementation Complexity of encoder/decoder

The requirements of very low error rate, very high throughput and low power architecture make the implementation of FEC sub system a non trivial issue. The Implementation can be divided in following two parts:

3.2.1 Encoder Implementation

Given that H matrix is sparse, the resultant generator matrix is generally not sparse. If no optimization procedure is incorporated in the encoder, it requires roughly $1/2 * (N - K) * K$ exclusive OR operations.

3.2.2 Decoder Implementation

Multi-Processor System-on-Chip (MPSoC) architectures are being widely investigated these last years in order to accommodate the increasing throughput and Flexibility requirements of emerging satellite broadcasting standards [12]. In multi-processor implementations several independent data blocks can be simultaneously decoded on different processors, this approach multiplies the costs (memories, area, and power consumption) along with the throughput. Typical decoder architecture will have 50 to 70 % memory component which is constituted mainly of channel memory and soft output intrinsic and extrinsic LLR. It should be noted that in a typical implementation, encoder complexity is less than 10 % of the complete codec design [13].

3.3 Code Design Parameters

Once the design metrices for system assessment are defined it is interesting to look at the physical design parameters of the FEC subsystem, which have either positive or negative effect on these metrices. Different parameters of FEC systems are as followings:

3.3.1 Code Length

For LDPC codes the smaller codeword length normally results in: Low implementation complexity, Low power consumption, and small latency. However these advantages come with relative performance degradation compared to large codes. Fig. 3 shows the relative bit error rate performance of a 16K and 4K LDPC code used in DVB-S2 and DVB RCS+M standards respectively. It could be seen that a using the smaller 4K code result in performance degradation of up to 1.4 dB with respect to 16K code length at a BER of 10^{-6}. Such performance degradation due to reduce code length could be improved to an extent using efficient code design techniques.

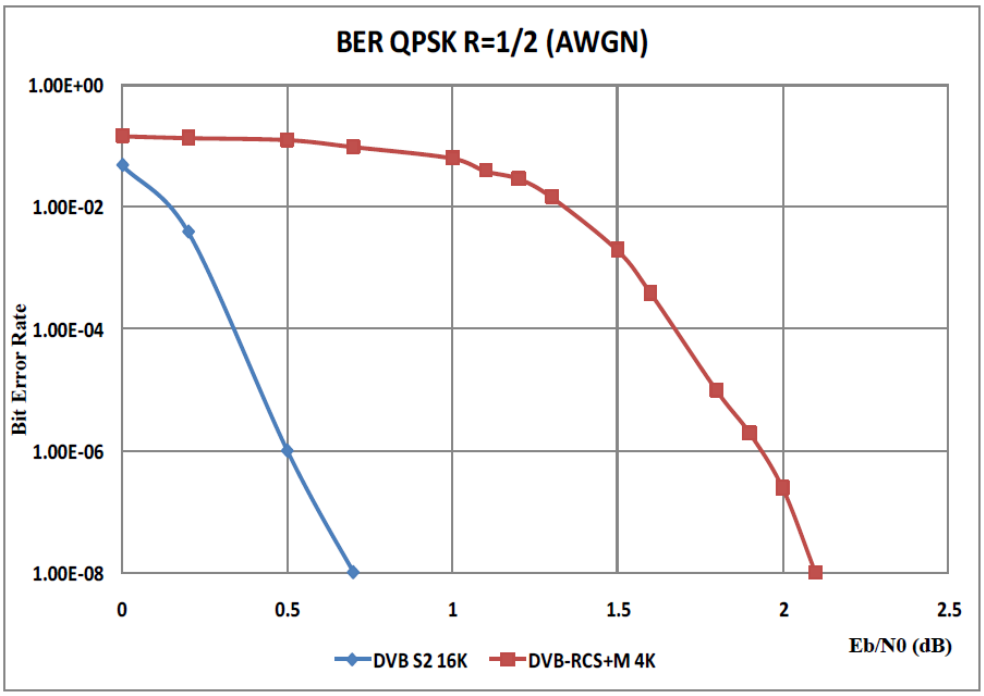

Figure 3. Impact of Code Length on Error Performance of the LDPC codes.

3.3.2 Code Construction (Matrix Structure)

Quasi-Cyclic structure in the information part, Staircase structure in the parity part: such constraint on code realization results in a significant complexity reduction of both encoder and decoder implementation, however with some performance degradation issues.

3.3.3 Code Concatenation

As mentioned previously, to improve the error correction performance of the LDPC codes a outer BCH code is concatenated to the LDPC code, which helps in lowering the error floor. If a *t* error correcting BCH is used, then the error floor lowers with increasing t, at the cost of a rate (throughput) penalty. The greater *t*, the better are the error floor performance, but the lower is the throughput. Additionally, the complexity of decoding the BCH at the receiver is not negligible (up to 15% of the total FEC decoding implementation) [13], and the complexity increases with the error correction capability *t*.

3.3.4 No. of Coding rates

Granularity of achievable error performances depends on the choices and number of coding rates. The implementation complexity of the system increases with increasing number of supported coding rates. In addition to it the system needs to be validated for multitude of such options, thus increasing the time to market.

4. Next Generation Short LDPC codes

Next generation satellite communication systems demand development of very short LDPC codes which have good error performance (BER = 10^{-10}), in addition have low complexity. In that context Navtel System has developed 4K NG (Next generation) codes, which give good error performance without the need of code concatenation (no BCH) thus low complexity. Table 1 shows a comparative analysis of the designed code parameters.

Table 1. Parameters for different 4K LDPC codes.

Parameters	DVB RCS+M [4]	Navtel's 4K NG LDPC
Block Length	4096	4050
Periodicity of Matrix	128	90
Supported Code Rates	1/4, 1/2, 3/4	1/4,1/3,1/2, 3/5, 2/3,3/4
BER	$10^{-7}/10^{-8}$	10^{-10}

4.1 Code Design Procedure

A protograph based code construction mechanism is used which was first introduced by [14]. The length of codeword for proposed code is N = 4050 coded bits, and the periodicity L = 90, the choice was based on their compatibility with existing LDPC codes in the DVBS2/T2 standards. This means that the base matrix of the protograph before lifting has N_b = 45 columns. The design procedure is composed of three main steps:

[Step1] First choose a very small base matrix filled with integers, the sum of integers represents the degree of each row/column. The matrix is of size M_{bs} x N_{bs}.

[Step2] Replace each integer by the same number of non-equal circulant matrices with minimum size L_1, such that $N_{bs}.L_1 \geq N_b$. Choose the circulants such that the girth is maximized. Then prune N_b-$N_{bs}.L_1$ columns of the obtained matrix H_b such that the number of columns is exactly N_b = 45. This pruning step changes the rate of the base matrix, and results in lower rates compared to the target rates.

[Step3] Use H_b as a protograph and perform lifting expansion with order L_2 = 90 to get the final parity check matrix H.

The three steps of the design procedure are highly interdependent, and require iterative tests to obtain the final matrices. This is because state of art code design methodologies doesn't allow relating the constraints that one can put on the 3 steps construction and the performance results of the final LDPC code. Once the parity check matrix is build, one need to check if the resulting parity check matrix has small trapping sets [11], which will be dominant in the error floor. For 4K NG codes, we have used techniques based on the algorithms presented in [15], [16]. The modified impulse algorithm is a very powerful technique to identify either small weight codeword or small weight trapping sets of sparse codes. We used the modified impulse algorithm to "reject" a designed LDPC if it has a small trapping distance. In the case where a construction is rejected, then one of the three steps ([Step1], [Step2], [Step3]) is changed to get another candidate LDPC code. The procedure

stops when the statistics of the minimum trapping distance is found sufficiently large.

4.2 Error Correction Performance

The code has been simulated for offset min sum based LDPC decoding, the error performance results for rate 1/2 code is shown in figure below along with the performance of similar code proposed in [4]. It can be seen that at a BER of 10^{-8} proposed 4K NG LDPC codes give approximately 0.5dB better performance than the corresponding codes in [4].

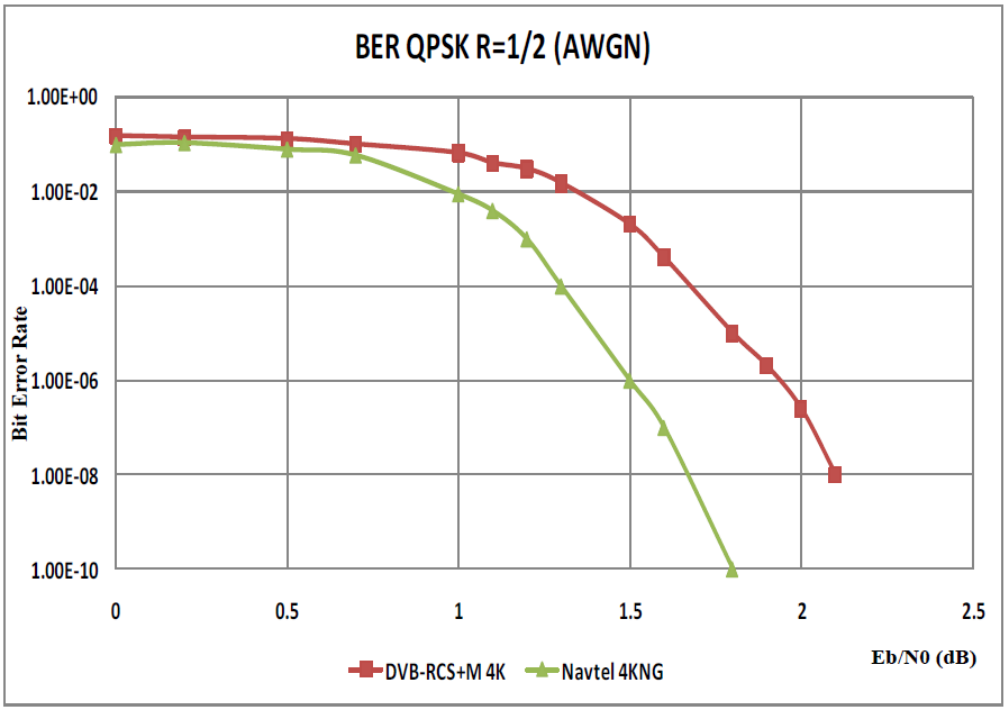

Figure 4. Error Performance of 4K NG LDPC code.

5. Conclusions

Low power FEC design involves the innovative ways of code design taking into account the different factor affecting the error performance of the code. By applying efficient code construction methods along with optimal choices of code block length and the periodicity of H matrix the goal of a low power FEC design can be realized. This paper presented a next generation 4K LDPC code designed for low power application in satellite communication domain which exhibits no error floors up to BER of 10^{-10}. Further optimization of the proposed code and innovative implementation techniques for low power consumptions are the next steps in this activity.

References

[1] DVB-S2, ETSI EN 302 307, V1.2.1, April 2009. At. http://www.etsi.org/deliver/etsi_en/302300_302399/302307/01.02.01_60/en_302307v010201p.pdf

[2] DVB-S2, ETSI EN 302 755 V1.1.1, Sept. 2009. At. http://www.etsi.org/deliver/etsi_en/302700_302799/302755/01.01.01_60/en_302755v010101p.pdf

[3] R. G. Gallager. 'Low-density parity-check codes'. IEEE Transactions on Information Theory, Pages 21-28, Jan. 1962. http://dx.doi.org/10.1109/TIT.1962.1057683

[4] G. Liva, M. Papaleo et al., "The Very Short Frame of Mobile DVB-RCS: Code Design and QoS Performance," International Journal of Satellite Communications and Networking (Wiley), Volume 8, Issue 5-6, September-December 2010. http://dx.doi.org/10.1002/sat.945

[5] "A Highly Flexible FEC Solution Offering Universally Good, Performance and High Speed Decoding", White Paper Oct. 2007. At http://www.trellisware.com/assets/pdfs/F-LDPC_Whitepaper.pdf

[6] T. Zhang and K. K. Parhi. Joint code and decoder design for implementation oriented (3;k)-regular ldpc codes. Signals, Systems and Computers, 2001. Conference Record of the Thirty-Fifth Asilomar Conference on , vol.2, pp.1232-1236 vol.2, Pacific Grove, CA, USA, 4-7 Nov. 2001. http://dx.doi.org/10.1109/ACSSC.2001.987687

[7] R. M. Tanner. A recursive approach to low complexity codes. IEEE Transactions on Information Theory, vol.27, no.5, pp. 533-547, Sep 1981.http://dx.doi.org/10.1109/TIT.1981.1056404

[8] M. Mansour and N. Shanbhag, "Low-power VLSI decoder architectures for LDPC codes," in Low Power Electronics and Design, 2002. ISLPED02. Proceedings of the 2002 International Symposium on, Monterey, USA, pp. 284 - 289, Aug. 2002. http://dx.doi.org/10.1109/LPE.2002.146756

[9] M. Fossorier, M. Mihaljevic, and H. Imai, "Reduced complexity iterative decoding of low-density parity check codes based on belief propagation," IEEE Transactions on communications, vol. 47, pp. 673 - 680, May 1999. http://dx.doi.org/10.1109/26.768759

[10] F. Guilloud, E. Boutillon, and J. Danger, "Lamda-Min Decoding Algorithm of Regular and Irregular LDPC Codes," in Proc. 3nd International Symposium on Turbo Codes and Related Topics, Brest, France, pp. 451 - 454, Sep. 2003.

[11] T. Richardson, "Error floors of LDPC codes", in the Proc. 41st Allerton Conf. Commun. Contr. Comput., pp. 1426 - 1435, Monticello, USA, September 2003.

[12] Frank Kienle, Torben Brack and Norbert Wehn, "A Synthesizable IP Core for DVB-S2 LDPC Code Decoding" Design, Automation and Test in Europe,2005. Proceedings , pp. 100-105 Vol. 3, Munich, Germany, 7-11 March 2005. http://dx.doi.org/10.1109/DATE.2005.39

[13] Datasheet FEC IPs, At http://www.navtelsystems.com.

[14] J. Thorpe, "Low-Density Parity-Check (LDPC) Codes Constructed from Protographs," JPL INP, Tech. Rep., Aug. 2003. http://ipnpr.jpl.nasa.gov/progress_report/42-154/154C.pdf

[15] D. Declercq and M. Fossorier, "Improved Impulse Method to Evaluate the Low Weight Profile of Sparse Binary Linear Codes", in the proc. of ISIT'08, Toronto, Canada, July 2008. http://dx.doi.org/10.1109/ISIT.2008.4595332

[16] S. Abu-Surra, D. Declerq, D. Divsalar, and W. Ryan, “Trapping Set Enumerators for Specific LDPC Codes”, in the ITA workshop, San Diego, CA, USA, February 2010. http://dx.doi.org/10.1109/ITA.2010.5454095