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A Low Settling Time Current-Mode Bandgap Reference Circuit for Low Noise Amplifiers

SARI MOHAN DAS* AND KOTA VENKATA RAMANAIAH

Department of Electronics and Communication Engineering, YSR Engineering College of Yogivemana University, Korrapadu Road, Proddatur – 516360, YSR District, Andhra Pradesh, India

In analog and mixed-signal circuit applications, the bandgap reference (BGR) circuit generates a reliable output. However, process, voltage, and temperature fluctuations all have an impact on output performance. Capacitors, resistors, and amplifiers increase the size of power supplies. As a result, the trimmer circuit is recommended for the BGR circuit to reduce fluctuations and process extension. Temperature compensation provides better temperature coefficients by adjusting the transistor voltage aspect ratio. The final characteristic curves are corrected to avoid slope variations, and temperature adjustment is required to provide the reference current in the BGR circuit. Temperature coefficients (TC) are calculated using electron mobility, voltage drop across the transistor, and threshold voltage factors. The temperature-dependent threshold voltage generates a low dependency drain current. Temperature reparation is achieved through temperature coefficients, and gate-source voltage is generated in the BGR circuit. Monte Carlo simulation beats efficient methods for identifying process variations and mismatches. Designing cascade current mirrors in the BGR circuit reduces the channel length modulation impact while increasing the resistance value. The trimmer current reference circuit outperforms the efficient reference current $21\mu A$ at time of 110 to 150 μS .

Keywords: Temperature coefficients, trimming circuit, bandgap reference circuit, transistors, and aspect ratio

*Corresponding author: E-mail address: mohantech418@gmail.com

1 INTRODUCTION

In the current mode BGR, the Proportional to Absolute Temperature (PTAT) and Complementary to Absolute Temperature (CTAT) voltages are converted into temperature-independent current, which is then utilized to generate a bandgap reference voltage. In the BGR circuit, 1.2V is considered the minimum supply voltage, and current mode BGRs are more adaptable. Temperature coefficients for BGRs based on bipolar junction transistors (BJTs) range from 20 to 100 ppm/C [1]. Temperature adjustment eliminates non-linear components, resulting in great accuracy and stability. To improve accuracy and stability, low-voltage BGRs use several curvature correction algorithms [2].

CMOS process advancement reduces feature size and lowers operating voltage. Temperature-compensated approaches are required to provide more precise reference voltages in BGR circuits [11]. BGR circuits are utilized in a variety of applications [12], including converters, linear regulators [15], and memory circuits that produce stable outputs in analog circuits. Furthermore, digital and analog circuits are integrated into the State of Charge (SoCs), resulting in noise and interference with the power supply. To minimize noisy chip environments, BGR circuits' primary side regulation (PSR) performance and precision must be improved [21]. Line sensitivity is diminished while the native oxide compensates for the voltage, which requires a higher supply voltage to operate.

In PTAT current generation, amplifiers are utilized to maintain system stability in bandgap voltage reference systems. The extra amplifiers increase the chip's area usage, as does the offset voltage, and noise interference lowers voltage difference accuracy. In analog or mixed-signal circuits, the temperature-independent current reference determines the steady bias current. The temperature compensation process takes place in a small range to increase the temperature coefficients (TC). Low dropout regulators (LDOs) require a high-quality, low-noise reference voltage to function properly. Furthermore, the BGR current is supplied as the input to the LDO, which employs the potential divider to convert the voltage and increase the noise performance.

1.1 Trimmer circuit

To give an accurate current reference, the trimmer circuit compensates for process fluctuations and mismatches. Transistors are linked in parallel with the switches in the trimmer circuit. The transistor values are modified by adjusting the aspect ratio, which accounts for temperature differences. The trimmer circuit, which modifies the final characteristic curves to reduce fluctuations and slop, improves the system's stability and accuracy. The sensitivity of the supply voltage is lowered by accounting for the temperatures utilized to generate the reference current. The transistor magnitude is modified to regulate the TC, lowering process deviations.

2 MOTIVATION

Branch currents are utilized to convey information in current mode circuits. However, the current mode circuit's construction technique has an effect on output accuracy. Because of the chip creation process, each produced circuit has a unique current reference. In electronic applications, supply voltage can vary for a variety of reasons.

2.1 Literature review

Zhi-Zhi Chenet et al. [21] proposed a supply rejection BGR circuit with a start up boost self-regulated topology. The boost structure increased the power supply rejection ratio (PSRR) and precision of reference current measurements. Monte Carlo simulations are used to obtain efficient findings that improve the performance of the BGR circuit. However, channel length should be optimized to reduce mismatches. Shichao Jia et.al [2] reported BGR with segmented temperature compensation, which created the compensation signal using the voltage differential between BJTs. In a wide temperature range, a low-temperature coefficient was attained, and simulations were offered to improve the performance. The approach provided improved stability and was mostly employed in low-voltage and power applications.

Furthermore, higher-order nonlinear currents were incorporated into the BGR circuits. Huanget al[6] demonstrated the gate leakage BGR circuit in biomedical applications. The reference voltage was generated using the PTAT and CTAT curves, which take use of the beta multiplier's body bias effect. Resistors were replaced with gate leakage transistors to ensure low power and area. The prominent circuits prevented offset difficulties, and the negative temperature caused sub-threshold leakage, which constrained the design.

2.2 Challenges

- Current mode. BGR has some limitations, including a lack of PTAT current supply, a broad consumption region, a high TC, and multiple operating points. However, the combined CTAT and PTAT performance was poor due to the poor performance of TC [10].
- The chopping procedure resulted in non-ideal input current and high-frequency noise for the operational amplifier (op-amp). In CMOS design, MOSFETs have lower temperature sensitivity and require several trimming points for accuracy.
- Recent reference source designs only meet very low TCs due to limited temperature characteristics affecting current generation. Higher order temperature residue terms existed in non-linear compensation BJTs, necessitating a more thorough elimination or rejection process [11].

3 PROPOSED BANDGAP REFERENCE CIRCUIT

To provide the reference current, the BGR circuit includes a starter circuit, a trimming circuit, n-Channel metal oxide semiconductor (NMOS), and PMOS transistors. Generation of I_{PTAT} and I_{CTAT} are added to generate the reference current. Then the trimming circuit is proposed across the reference current generation area, which is used to eliminate the process variations. The trimming circuit reduces process errors while changing the size of resistance to regulate the voltage TC. Figure 1 shows the schematic diagram for the proposed methodology.

The startup circuit shown in figure 2 is utilized to maintain a stable condition and is located between the circuit's input and output of the feedback path. When the output voltage drops below the threshold, the startup circuit applies voltage to the input. In this starter circuit, the bandgap reference is monitored using capacitive coupling. The beta multiplier circuits are then connected to the starter circuit, which provides the PTAT and CTAT currents. The CTAT's nature is regulated by adjusting the aspect ratio, and the beta multiplier circuits are intended to compensate.

Low voltage. CR combines the PTAT and CTAT currents to provide the temperature-compensated reference current. The resistive design CR creates the additional voltage that powers the transistors and operates in the sub-threshold region. This design assures low power operation, and the

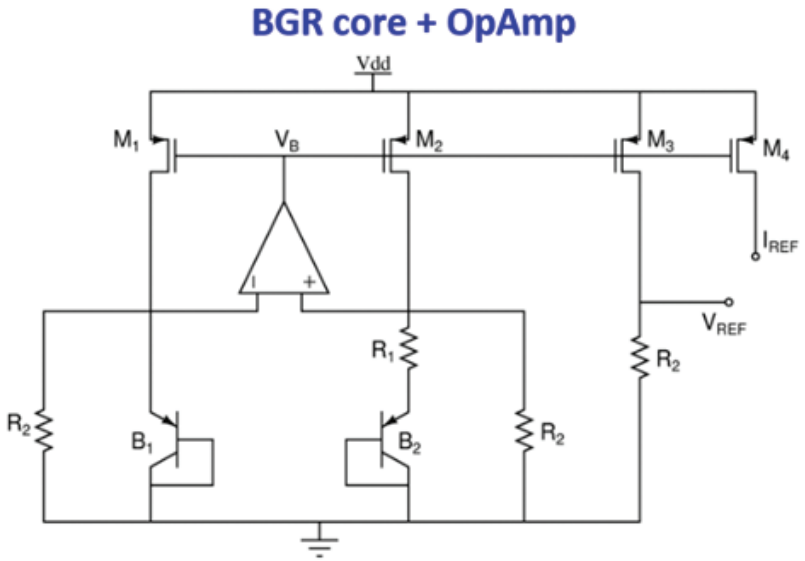

FIGURE 1
Schematic of the proposed BGR circuit

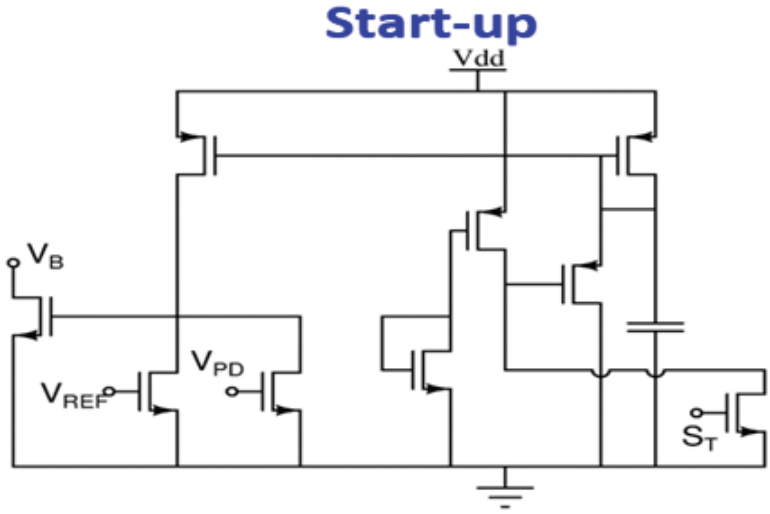

FIGURE 2
Schematic diagram of the startup circuit

mathematical expression for the drain-source current and resistance is as follows:

$$i_{ds} = \frac{X}{J}\mu_n c_o (s-1) v_t^2 e^{\frac{v_{gs}-v_{th}}{nV_t}} \left(1 - e^{\frac{-v_{ds}}{v_t}}\right) \tag{1}$$

$$r_{ds} = \frac{\boldsymbol{v_t}\left(\boldsymbol{e}^{\frac{\boldsymbol{v_{ds}}}{\boldsymbol{v_t}}} - 1\right)}{\boldsymbol{i_{ds}}} \tag{2}$$

Where $\frac{X}{J}$ is indicates an aspect ratio, mobility is denoted as the μ_n, c_o is the capacitance, thermal voltage is represented as a v_t gate-source voltage is represented as v_{gs}. i_{ds} is the drain-source current, r_{ds} is the drain-source resistance, v_{ds} is the drain-source voltage and n is the slope of sub-threshold. Then the PTAT current is formed by connecting the resistance r4 between the source voltages, and the mathematical expression for the PTAT current is followed as,

$$I_{PTAT} = \frac{nv_t \ln(j)}{r_3} \frac{1}{1 - \left(\frac{\phi}{2\sqrt{\varphi_s}}\right)} \tag{3}$$

Where I_{PTAT} represents the PTAT current, ϕ is the body bias coefficient, φ_s is the surface potential. Line regulation effects are enhanced by lowering channel length modulation effects. The PTAT voltage is determined by means of the current, resistor, and gate-source voltages.

$$I_1 = \frac{v_{gs1} - v_{gs2}}{r_1} \tag{4}$$

And the temperature dependence PTAT current expression is as follows,

$$\frac{\partial I_{PTAT}}{\partial t} = I_{PTAT}\left(\frac{1}{t} - \frac{1}{r_3}\frac{\partial r_2}{\partial t}\right) \tag{5}$$

Where $\frac{\partial I_{PTAT}}{\partial t}$ is the temperature dependence of PTAT current and the temperature is represented as *t*. CTAT behaviors are controlled by two MOS transistors with varying channel lengths and threshold voltages. In this design, the CTAT current is generated using the Gate source voltage. This circuit utilizes low occupied silicon area, and the mathematical expression for the current is as follows:

$$I_{r1} = \frac{v_{gs}}{r_1} \tag{6}$$

CTAT current flows through the resistance and then the mathematical expression for the first-order TC is derived as follows,

$$I_{CTAT} = \frac{v_g}{r_2} \tag{7}$$

$$\frac{\partial I_{CTAT}}{\partial t} = \frac{1}{r_2}\frac{\partial v_g}{\partial t} - \frac{I_{CTAT}}{r_2}\frac{\partial r_2}{\partial t} \tag{8}$$

The reference current is determined by the threshold slope, the poly resistors, and the threshold voltage. The shared resistive path can yield compensated voltage drops, and the mathematical model of the expression is derived.

$$V_{sub} = \left(I_{PTAT} + I_{CTAT}\right) r_3 \tag{9}$$

3.1 Current reference

The CR circuit offers precise current and is commonly found in analog and mixed-signal systems. The reliance of current mirror performance is minimized by altering IC calibration, temperature, and supply voltage. The voltage reference circuit generates the reference voltage, and the resistor is integrated into the circuit. The current reference circuit removes temperature and supply changes, which are dependent on the voltage reference circuit.

$$I_{ref} = \frac{v_{dd} - v_{gs2} - I_0 r_2}{r_1} \tag{10}$$

Where v_{dd} is supply voltage, v_{gs} is gate-source voltage, r and is resistance.

3.2 Temperature dependence

Operating temperature is regarded as an essential component in the electrical characteristics of electronic circuits. Temperature and power supply variations affect the MOS transistors in the BGR circuit. The PTAT current increases linearly with temperature, whereas the CTAT current decreases linearly with temperature. There are mismatches and variances here, so temperature correction is essential for the circuits to compensate for the temperature and generate the reference current.

3.3 Temperature compensated current reference

The voltage drop across the resistor determines the sum of two temperature coefficients that are opposing. The first TC is based on the transistor overdrive voltage, which had a positive temperature due to electron mobility. The temperature dependence of threshold voltage is negative, and low temperature coefficients are calculated using the ratios. The opposite temperature coefficients are balanced, which is employed to operate the circuit reference. The transistors' aspect ratio is utilized to correct for the PTAT and CTAT currents and generate the reference current.

$$I_{ref} = \beta_1 I_{PTAT} + \beta_2 I_{CTAT} \tag{11}$$

Where β_1 and β_2 are the temperature coefficients. Temperature coefficients should be compensated to generate the current reference in the circuit topology.

4 RESULTS AND DISCUSSION

Process & Temperature Sims (post-pex)

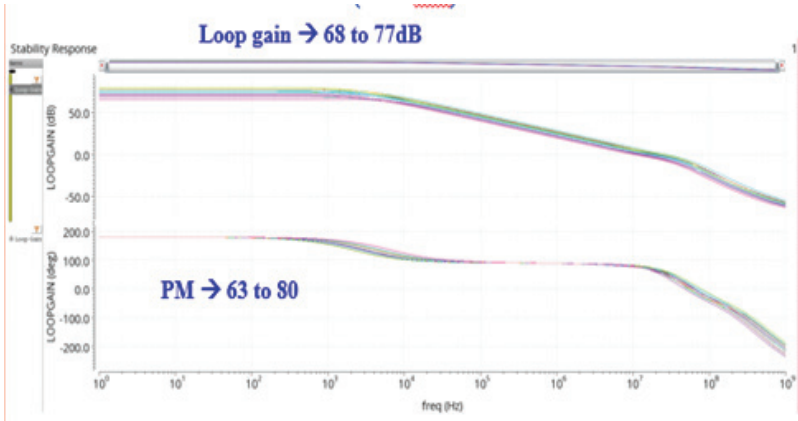

FIGURE 3
Stability Analysis (Gain and Phase margin) of BGR loop

Stability Summary - circuit "tb_CDA_BGR" with loop probe "I1.IPRB0"
@100fF load

modelFiles	temperature	PM(deg)	@Freq(Hz)	GM(dB)	@Freq(Hz)	
"design_wrapper.lib.scs:sf_pre"	-40	63.612	24.562M	11.173	64.639M	
"design_wrapper.lib.scs:sf_pre"	25	69.979	17.558M	13.598	60.293M	
"design_wrapper.lib.scs:sf_pre"	125	75.687	12.004M	16.033	54.281M	
"design_wrapper.lib.scs:fs_pre"	-40	66.39	23.953M	11.405	66.065M	
"design_wrapper.lib.scs:fs_pre"	25	72.086	17.058M	13.823	61.438M	
"design_wrapper.lib.scs:fs_pre"	125	77.216	11.64M	16.272	55.16M	
"design_wrapper.lib.scs:ff_pre"	-40	63.248	26.307M	12.762	79.008M	
"design_wrapper.lib.scs:ff_pre"	25	67.736	19.398M	14.894	72.691M	
"design_wrapper.lib.scs:ff_pre"	125	73.055	13.569M	17.026	64.337M	
"design_wrapper.lib.scs:ss_pre"	-40	65.921	22.828M	10.096	55.739M	
"design_wrapper.lib.scs:ss_pre"	25	74.228	15.658M	12.713	52.317M	
"design_wrapper.lib.scs:ss_pre"	125	80.063	10.38M	15.331	47.411M	
"design_wrapper.lib.scs:tt_pre"	-40	64.892	24.267M	11.288	65.269M	
"design_wrapper.lib.scs:tt_pre"	25	70.943	17.318M	13.709	60.793M	
"design_wrapper.lib.scs:tt_pre"	125	76.369	11.832M	16.147	54.645M	

FIGURE 4
Phase margin, phase margin frequency, gain margin and gain margin frequency across PVT at 100fF load

Stability Summary - circuit "tb_CDA_BGR" with loop probe "I1.IPRB0"
@40pF load

modelFiles	temperature	PM(deg)	@Freq(Hz)	GM(dB)	@Freq(Hz)	
"design_wrapper.lib.scs:sf_pre"	-40	63.599	24.57M	11.17	64.632M	
"design_wrapper.lib.scs:sf_pre"	25	69.97	17.563M	13.595	60.288M	
"design_wrapper.lib.scs:sf_pre"	125	75.682	12.007M	16.031	54.276M	
"design_wrapper.lib.scs:fs_pre"	-40	66.378	23.96M	11.403	66.058M	
"design_wrapper.lib.scs:fs_pre"	25	72.079	17.063M	13.821	61.432M	
"design_wrapper.lib.scs:fs_pre"	125	77.213	11.643M	16.269	55.156M	
"design_wrapper.lib.scs:ff_pre"	-40	63.238	26.314M	12.76	78.999M	
"design_wrapper.lib.scs:ff_pre"	25	67.728	19.403M	14.891	72.682M	
"design_wrapper.lib.scs:ff_pre"	125	73.05	13.573M	17.024	64.331M	
"design_wrapper.lib.scs:ss_pre"	-40	65.905	22.836M	10.093	55.733M	
"design_wrapper.lib.scs:ss_pre"	25	74.22	15.663M	12.711	52.313M	
"design_wrapper.lib.scs:ss_pre"	125	80.06	10.383M	15.328	47.408M	
"design_wrapper.lib.scs:tt_pre"	-40	64.879	24.274M	11.285	65.263M	
"design_wrapper.lib.scs:tt_pre"	25	70.935	17.323M	13.706	60.787M	
"design_wrapper.lib.scs:tt_pre"	125	76.364	11.835M	16.144	54.64M	

FIGURE 5
Phase margin, phase margin frequency, gain margin and gain margin frequency across PVT at 40pF load

DC Simulation (post-pex)

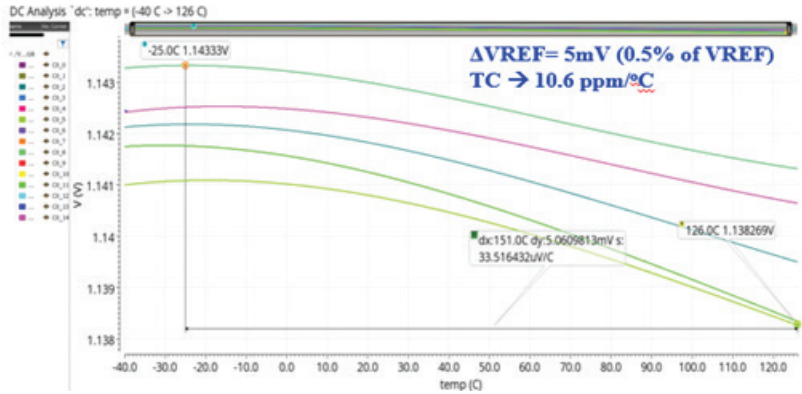

FIGURE 6
BGR reference voltage and Temperature coefficient across PVT

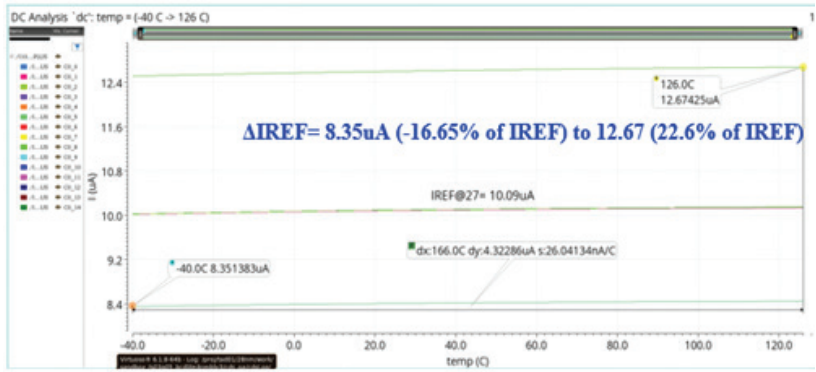

FIGURE 7
Reference current across PVT

Transient Simulation (post-pex)

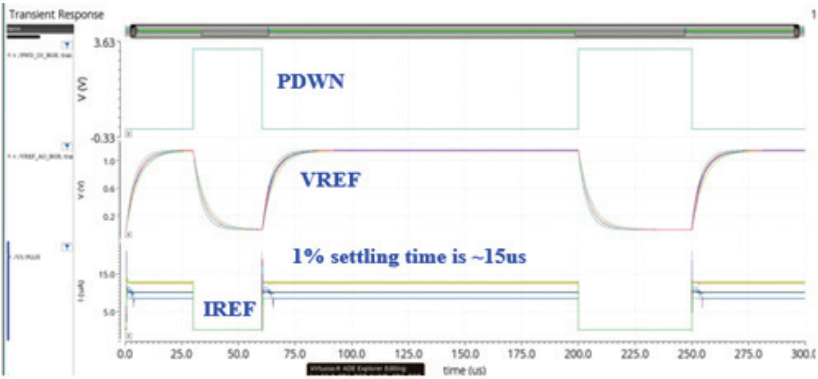

FIGURE 8
Sequencer and startup mechanism of BGR across PVT

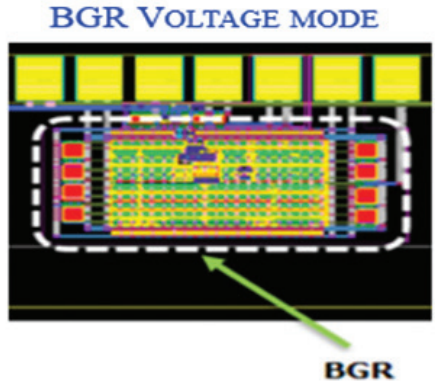

FIGURE 9
The layout of BGR with start-up circuit

4.1 Monte Carlo simulation

A Monte Carlo simulation's probabilistic model adds elements of uncertainty or randomness to aid in prediction. In this simulation, the probabilistic model produces distinct results. The mean is 1.14237, while the standard deviation is 24.6765. Figure **24** illustrates the Monte Carlo simulation. When adjusting the voltage reference, an offset value is utilized to determine precise detection, and the voltage range is extended from 0 to millivolts. According to the simulation results, the initial sample count yields 700mV. At a sample count of 100, the voltage range is 740mV to 760mV. The voltage range is then reduced within the sample count range as the temperature rises.

Monte Carlo Simulation (post-pex)

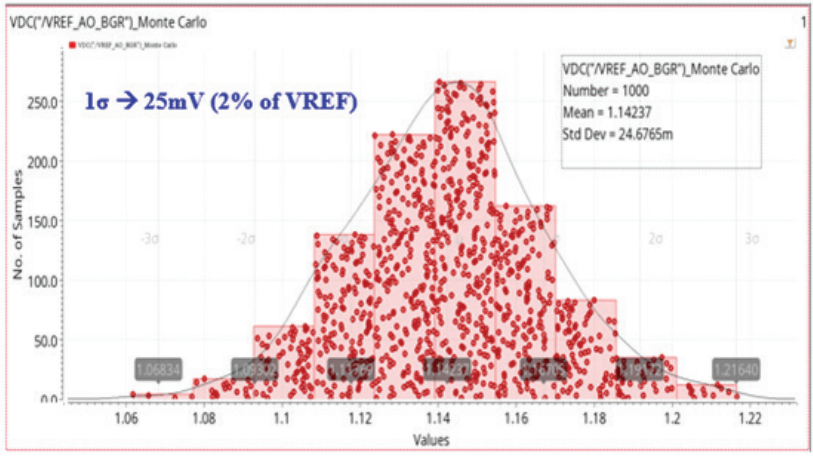

FIGURE 10
Monte Carlo simulation of Reference Voltage

DC Simulation (post-pex)

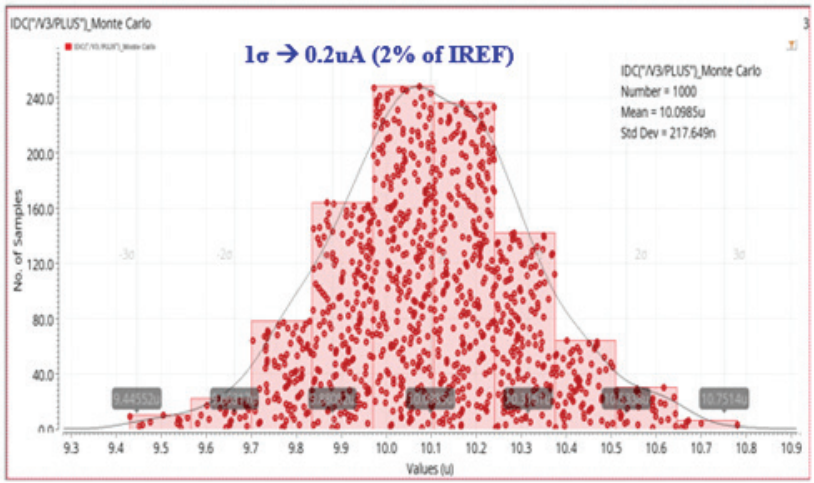

FIGURE 11
Monte Carlo simulation of Reference Current

Measured data

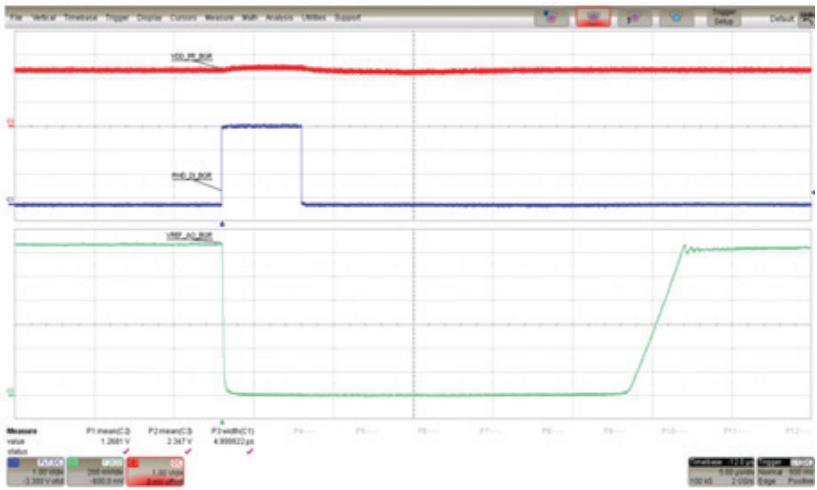

FIGURE 12
Measured results of BGR

5 CONCLUSION

Bandgap reference output fluctuates between chips due to process changes, and process parameters only control the bipolar bandgap reference principal effect by 15% or 40%. As a result, this problem emerges due to the use of

various types of semiconductor resistors. Due to process variances and mismatches, the circuit exhibits varying voltages and curvature. To prevent fluctuations and process expansions, the BGR circuit includes a trimmer circuit. The aspect ratio of the transistor voltage is changed to offer compensatory temperatures. Slope fluctuations are removed by adjusting for temperature, and reference current is provided by using superior TCs in the circuit.

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